REMARKS

This amendment is submitted in response to the office action of 16 May 2006 which considered pending claims 1-9 and 11-18. Pending claim 10 was not examined for reasons unknown and not stated. Independent claims 1-4 and 17 were rejected under 35 U.S.C. 102 (e). This office action also rejected dependent claims 5-9, 11-16, and 18 under 35 U.S.C. 103a. The present amendment revises claims 1, 2, 14, 17, and 18; and resubmits claims all claims (1-18) for reconsideration.

As per Claim Objections in paragraph 3. On page 2 of the office action: typos in claims 1, 2, 14, and 18 have been corrected.

As per Claim Rejections 35 U.S.C. 112. In paragraph 5 of the office action: Claims 1, 2, and 17 recited "defines an interface" whose meaning the examiner asserted he could not understand. This term has been changed to "is an interface" in claims 1, 2, and 17 to facilitate the examiner's understanding.

The undersigned asserts that the meaning of "defines an interface" is replete with clarity and exactitude and devoid of ambiguity or uncertainty. The term is commonly used in the English language. The undersigned has used the term "defines ...." for many years in practice before the USPTO. No examiner has priorly objected. The above office action is the first time an objection has been encountered asserting that the meaning of the term " defines ....." cannot be understood. It would have been helpful if the examiner had stated exactly what he does not understand. The examiner is respectfully referred to an English dictionary where the meaning of the term "defines" is set forth with specificity.

Since this term is commonly used in the English language and is free from ambiguity, no change is being made in the specification to insert a definition of a commonly used term that should be understandable to all.

In paragraph 7 on page 3 of the office action the examiner continues with his comments regarding the use of "defines an interface". In so doing he states

> ..."It is not clear if the claim language of "said access flow regulator define an interface between" sets forth that the access flow indicator is an interface between the router and memory management system

or configured an interface between said router and the memory management system."

The applicant cannot respond to the above quote other than to state that he has no idea what the examiner is talking about, or what question the examiner is asking, or what issues are raised by the quote. The applicant will be happy to respond to the query if the examiner repeats his question or using improved grammar.

Request for the receipt of an advisory action together with the withdrawal of the final office action of 16 May 2006.

It is respectfully asserted that the final office action of 16 May 2006 failed to respond to the applicant's amendment of 28 February 2006. In particular, the office action of 16 May 2006 failed to act upon to the claims as revised by the 28 February 2006 amendment. The claim analysis provided in the office action of 16 May 2006 apparently analyzes the wrong claims set; namely, the claims as they existed prior to their being amended by the 28 February 2006 amendment. The changes made by the 28 February 2006 amendment further distinguish the claimed invention from Ferguson. The applicant's amendment of 28 February 2006 revised independent claims 1 and 2 by inserting language, which now states, in essence, that the access flow rate regulator defines an interface between a fileserver and a memory management system. The examiner's claim analysis in the office action of 16 May 2006 disregarded the claim changes made regarding the claimed interface by the 28 February 2006 amendment. As a result, the examiner's comments and claim analysis made in the 16 May 2006 office action are of no value. This failure by the examiner is a serious error and has prejudiced the applicant's right to receive an office action that acts upon the claims as amended by the 28 February 2006 amendment. These claims changes are meaningful and material to the prosecution of this application.

The applicant respectfully requests that the office action of 16 May 2006 be set aside and that the examiner provide the applicant with a replacement office action that acts upon the claims as amended both by the 28 February 2006 amendment as well as by this present amendment. The present amendment makes minor changes to independent claims 1,2,17 based upon the examiner's inability to understand the term "defines an interface" which was inserted into the application by the amendment of February 28, 2006. This allegedly objectionable term has been removed from the claims and has been replaced by the term "is an interface" in hopes of facilitating the examiner's understanding of the claimed invention.

In summary, because of the examiner's apparent error in failing to act upon the correct claim set in the final office action of 16 May 2006, it is requested that the examiner respond to this present amendment, with an advisory action, which grants the applicant time to continue normal prosecution and time to respond to any further actions taken by the examiner.

It is hoped in the furtherance of justice and fair play, that the examiner will be able to grant the applicant's request for an advisory office action. This requested advisory office action will for the first time provide the applicant with the right to which he is entitled, namely the right to have the claims acted upon in a timely manner based upon the current status of the claims.

It cannot be asserted that the 16 May 2006 office action acted upon the amended claims. A review of the examiner's analysis for independent claims 1 and 2 indicates that the claim changes made by the 28 February 2006 amendment were not mentioned by the examiner. If this statement should be disputed, the applicant hereby requests a clarified claim analysis that addresses the status of the claims as revised by the 28 February 2006 amendment. The claim changes to be addressed include the changes which state, in essence, that the access flow regulator is an interface between the file server and the memory management system. The applicant requests

that, as required by a 35 U.S.C. 102 rejection, the examiner point out with specificity and particularity where Ferguson discloses and discusses an access flow regulator that is an interface between a file server of Ferguson and a memory management system of Ferguson.

It is hoped that that the examiner has the freedom to grant the applicant's request for an advisory office action. However, in the event that the examiner is unable or unwilling to grant applicant's request, it is respectfully requested that this matter be referred as a petition to the division director together with reasons indicating why the applicant believes he is entitled to relief which, for the first time, will grant him the right to receive an office action that acts upon with particularity and specificity the applicant's claims as currently amended.

Discussion of the disclosure of the present application and Ferguson et al (US 6, 79 8,777)

Applicant's disclosure

The present application discloses a memory management system that provides memory storage facilities for a fileserver that is separate from the memory management system and that is coupled to the memory management system by an access flow regulator that functions as an interface between the fileserver and the memory management system. The memory management system provides memory storage facilities for all data files received by ports of the file server. These memory storage facilities are common to all ports of the file server. In other words, the applicant's memory management system may be considered to be a stand-alone or separate memory facility that provides for the storage of all data files received by ports of the file server. This eliminates or reduces the need for the provision memory storage in ports of the fileserver.

The provision of the common memory storage by a memory management system it is advantageous in that it illuminates the need of the prior art arrangements

which required memory storage in the file server ports. The provision of memory storage facilities in the file server ports required that each port of the file server be provided with an adequately sized memory so that incoming data files would are not dropped. This arrangement is costly and complex since all ports do not serve the same level of incoming traffic. It is therefore difficult to determine in advance the memory size required by each port. Also, the traffic level of the various ports could vary with time. It is therefore it was necessary to equip each port with a memory size adequate for the busy condition of the port even though the provided memories are not be utilized during low traffic conditions of a port.

The memory management system of the present disclosure overcomes the disadvantages of the prior art arrangements by providing memory storage facilities that are common to all ports of the file server. This eliminates the need for the provision of separate memory facilities in the fileserver including separate and appropriately sized memory facilities in each port of the fileserver.

The access flow regulator is a key element in applicant's system. The access flow regulator functions as an interface between the ports of the file server and the memory management system. The access flow regulator performs many functions in applicant's disclosure. It functions to receive requests from the ports of the file server for the storage of data files received by the ports. Upon receiving such requests, the access flow regulator determines the availability of an idle memory in the memory management system and. Having determined that a memory is available, the access flow regulator transmit signals to control circuitry associated with the selected memory to cause the receive data file to be written into the selected memory.

The access flow regulator is also operable to receive a read request from a port circuit for the readout of a data file stored in the memory management system. The access flow regulator receives a read request, identifies the memory currently storing the data file identified by the received read request, and controls the circuitry of the memory management system to read out the requested data file. The data file that is read out is that extended through the access flow regulator to an output port of the file server.

The memory storage facilities of the memory management system are disclosed on figure 18. These memory facilities comprise high-speed low capacity RAMs 1803 and further comprise lower speed bulk memory embodied in a remote RAM 1806. The high-speed RAMs 1803 are involved on each write operation as well as on each read operation. On write operations, the received data file is written into a RAM 1803 up to the limited storage capacity of the ram. When the limited storage capacity of the RAM is exceeded, the RAM transfers its current contents to bulk memory 1806 and continues to receive further portions of the received data file. This operation continues until the entirety of the received data file is stored. At that time, and depending upon the size of the received file, a small portion of the data file is stored in the receiving RAM 1803 while the remainder of the receive file is stored in remote RAM 1806.

The process works in reverse for read operations. On read operations, the portion of the selected data file currently stored in RAM 1803 is read out and applied to the access flow regulator 1801. At the same time, the access flow regulator controls the operation of the memories 1803 and 1806 so that the remainder of the requested data file is read out of remote bulk RAM 1806, temporarily stored in high speed RAM 1803, and then extended to access flow regulator 1801 for transmission to an output port of the file server. The provision of both high-speed low capacity memories 1803 and lower speed bulk memories 1806 permits the memory management system to store data at high speeds while providing for the storage of the data in lower cost bulk memories comprising remote RAM 1806.

Ferguson disclosure

The Ferguson disclosure is as different from the applicant's disclosure as night is from day. Ferguson does not disclose an independent memory system that is separated from a file server by an access flow regulator comprising an interface. Instead, Ferguson discloses a fileserver comprising a router that receives incoming packets on input ports of the router and extends the received packets to appropriate output ports of the router. Ferguson requires memory facilities in the ports of his router so that the received packets are extended in a timely manner to the proper output

ports. The required memory facilities are entirely contained within the Ferguson router and are distributed among the ports so that each port is served by a memory having the storage capacity adequate for the input port to serve incoming traffic.

Ferguson discloses a memory 104 on figure 2B that is common to a plurality of ports. Ferguson also discloses memory in each port, such as port 150 on figure 3. The common memory 104 and the memory required in each port presumably cooperate so that the incoming packets are timely routed to the appropriate output port. The most that can be said for Ferguson, in so far as the present discussion is concerned, is that Ferguson discloses both common memory as well as memory provided on a per port basis. To this extent, Ferguson might possibly be an improvement over the typical prior art such as that shown on figures 1A and 1B of Ferguson where the memories are provided entirely on a per port basis.

While Ferguson might possibly use memory more efficiently than that of the prior art shown on his figures 1A and 1B, it cannot possibly be construed as being comparable to applicant's disclosure wherein a stand-alone memory management system is provided that is common to all ports of a file server and that uses an access flow regulator as an interface between a file server and the memory management system. All data files received by the ports of applicant's fileserver are extended through access slow regulator to memory facilities of the independent memory management facility.

On a more detailed level, the memory facilities of Ferguson do not comprise a high-speed low capacity memory that receives all data files and that uses a lower speed high-capacity bulk memory for overflow of the received data that exceeds the limited storage capacity of the high-speed low capacity memory. Port 150 on figure 3 of Ferguson discloses head and tail buffer memory 318 and a memory 105 entitled global data area memory bank and further discloses bulk memory 319.

Contrary to the examiner's assertion in the office action of 16 May 2006, memories 318 and 105 of Ferguson are not comparable to and do not function in the manner comparable to that of applicant's high-speed memory 1803 and low speed bulk memory 1806 shown on applicant's figure 18. Memory 318 of Ferguson may be of the high-speed low capacity type that receives the head and tail of a packet. However,

memory 318 of Ferguson does not receive the entire packet. Ferguson also does not store a small portion of the received packet in memory 318 while passing the excess portion of the received packet to global memory 105 for storage in memory 319 the portion of the excess portion that exceeds the capacity of the high-speed low capacity memory 318.

Thus, the examiner is in error when he applies the Ferguson memories 318 and 105 of figure 3 of Ferguson to the applicant's independent claims, such as claim 1. The last two elements of applicant's claim 1, in essence, recite the steps of writing both the first part and excess portion of a data file into the high-speed memory and transferring the excess portion of the data file from the high-speed memory to the bulk memory while leaving the first portion of the data file in the high-speed memory. It should be obvious to one skilled in the art who understands both the applicant's disclosure and Ferguson that the Ferguson memories 318 and 105 of Ferguson's figure 3 do not function in the manner applicant's high-speed memories 1803 and bulk memories 1806 function to cooperatively store large data files.

In summary of the foregoing analysis of applicant's disclosure and Ferguson it should be apparent to those skilled in the art that Ferguson does not anticipate or make obvious applicant's claims.

The disclosure of Ferguson is non-enabling with respect to the applicant's claimed invention.

It is respectfully requested that the Ferguson patent be declared to be non-enabling with respect to the applicant's claimed invention. Ferguson has been studied in detail and it is submitted that the portion of the Ferguson disclosure (Figures 2B and 3) that the examiner apparently considers to be relevant and material to applicant's claims is confusing, poorly documented and explained. A major element of Ferguson described by his text, but it is not shown on figure 2B. The text regarding the operation of his figure 2B describes a major element (150) that is not shown on figure 2B. As a result, the Ferguson disclosure cannot be understood.

Figure to 2B of Ferguson is a high-level system diagram. Some of the elements shown on figure 2B are described in the text in a manner and detail appropriate for an

understanding of the high-level concepts of the router element of figure 2B. However, shortly into the description of figure 2B the Ferguson text beginning on column 5 begins a detailed and prolonged description of a "multifunction multiport 150" whose understanding is crucial to an understanding of Ferguson but which is not shown on Ferguson figure 2B. This is a significant error that makes an understanding of Ferguson impossible. The Ferguson system of figure 2B it is incomplete as shown and cannot be understood without the missing "multifunction multiport 150" which is shown in Figure 3.

The multifunction multiport 150 that is missing from figure 2B is shown in detail on figure 3. However, the disclosure on figure 3 is incomplete and inadequate since it fails to indicate how the multifunction multiport 150 of figure 3 can be connected to the system of figure 2B. Some of the interface conductor paths on figure 3 are sufficiently understandable to enable one's skilled in the art to guess the element of figure 2B to which the conductor path of Figure 3 should be connected. Examples of such conductor paths on figure 3 are element 304 (shown on the lower left of figure 3), which is designated as the "input switch 100" path to which element 304 should be connected on Figure 2B. The same may be said for element 305 shown at the top of figure 3. The same may be said for element 316 having the conductor path designation "output switch 102". The same cannot be said for element 300 having the "line input" path designation. The same cannot be said for element 308 having the "line output" designation. The text for Figure 3 describes element 300 as receiving input packets. One can only guess how the system's shown on figure 2B receives an input packet and applies the packet to element 300 on figure 3. The same may be said for element 308 and its path designated as a "line output".

On a more detailed level, Ferguson states that his memory element 318 receives and stores the head and tail portion of a buffer while the notification area 319 stores the remainder of the buffer whose head and tail is stored in memory 318. Also, it is not understood how an input packet received by element 300 is subdivided into head and tail portion and stored in memory 318 while the remainder of the buffer is stored in notification area 319.

The function of the Ferguson router is to receive an input packet and promptly extend the packet to the correct output of the router. In so doing, the router must expeditiously perform necessary processing of the packet and extend it to the appropriate output of the router. It should be obvious to one skilled in the art that the Ferguson memories that temporarily store the packets are provided on a per port basis. These memories on figure 3 are memory 318, which stores the head and tail portion of the buffer and memory 319, which stores the remainder of the buffer. The examiner has admitted during the prosecution of the application that the Ferguson memories are provided on a per port basis. The applicant's invention differs from Ferguson in that the applicant discloses a memory management system that operates on a stand-alone basis of to store data files of a file server to which the memory management system is connected via an access flow regulator which functions as an interface between the memories of the memory management system and a file server.

Another distinction between applicant's invention and Ferguson is that Ferguson uses memory 318 to store head and tail portion of buffer and to separately store the remaining portion of buffer in memory 319. So far as can be determined from Ferguson, his memories 318 and 319 on Figure 3 do not communicate with each other and do not transfer the contents of buffers between each other. The applicant's invention, by contrast, provides high-speed low capacity memories together with a low-speed large capacity bulk memory to store data files that are extended by a file server via the applicant's access flow regulator to the applicant stand-alone memory management system for the storage of the receive data files. On write operations, a receive data file is extended by the access flow regulator to a selected high-speed low capacity memory which stores a first portion of the data file and transfers the excess portion of the data file to the bulk memory. The process works in reverse on a read operation when the selected data file is a read out of the bulk memory to the high-speed memory storing the first portion. The high-speed memory con currently transfers the first portion together with the excess portion to the access flow regulator, which further extends both portions of the data file to the file server. It can be seen from the foregoing that the applicant's use of a high-speed memory together with a bulk memory which stores access information of the data file received from the high-speed

memory is as different from Ferguson as night as different from day. Ferguson's memories 318 and 319 do not transfer packets between each other as do applicant's memories 1803 and 1806.

The applicant's use of an access flow regulator comprising an interface and the use of a high-speed memory and a low-speed memory together in a cooperative basis is not shown on by Ferguson. The details that distinguish Ferguson from the applicant's invention relate to material on Figures 2B and 3 of Ferguson. This missing information precludes an understanding of Ferguson's Figures 2B and 3.

It is therefore submitted that the portions of the Ferguson (Figures 2B and 3) relied on by the examiner cannot be understood because of Ferguson's failure to describe his multifunction multiport 150 with specificity and clarity so that one's skilled in the art can understand the Ferguson material.

It is therefore respectfully requested that Ferguson be considered to be non-enabling on the grounds that figures 2B and 3 of Ferguson cannot be understood by one skilled in art to which Ferguson pertains. Consequently, it cannot be said that Ferguson teaches anything regarding Figures 2B and 3 that that can be understood.

35 U.S.C. 102(e) rejections.

The applicant respectfully traverses the 35 U.S.C. 102 (e) rejections of Independent claims 1, 2, and 17 as well as applicant's dependent claims 3 and 4. The examiner's attention is respectfully directed to the previously discussed material regarding the present invention and the Ferguson disclosure. This priorly discussed material eliminates the need for a repeated discussion of the same material for each of the following discussed rejected claims. The examiner's familiarity with his prior material is assumed in connection with the following discussion of the rejected claims.

Re: rejection of independent claim 1. In paragraph 3 on page 4 of the office action, the examiner sets forth his reasoning for the rejection of claim 1 over Ferguson. The applicant traverses this rejection. The examiner's statement is replete with errors. First of all, as shown on page 18 of the present application, server 1811, access flow regulator 1801, and the memory management system are separate devices. The memory management system and its memories are shown on the lower portion of

figure 8 as comprising memories 1803 and 1806 and associated apparatus such as background access multiplexer 1808 and access flow regulator 1801. Access flow regulator is an interface between the server port circuits 1817, 1818 and the memory management system. The memory management system includes the high-speed RAM bank memories 1803 and the remote RAM 1806 shown on the lower portion of figure 18. Ferguson does not show any comparable relationship between port circuits, an access flow regulator and both high-speed and low-speed memories that are common to all port circuits The Examiner failed to recognize this claimed relationship in is rejection of claims 1, 2, and 17.

This relationship is crucial to the applicant's invention since it allows the applicant's memory system to function essentially as a standalone entity while serving the storage needs of all ports 1817, 1818 of fileserver 1811. Ferguson shows no such relationship. Ferguson does not disclose memory facilities common to all ports of his system. Ferguson does not disclose a common group of both high-speed memories and low-speed bulk memories which function to store data files received by ports of his system. Ferguson does not extended data files received by his ports to his memories via an access regulator functioning as an interface between all of the ports and the memories of a memory management system common to all ports. The examiner is correct when he states in his remark that the Ferguson queues (memories) are implemented on a per port basis. It is not understood how the examiner, knowing the deficiencies of Ferguson , could assert that Ferguson anticipates the applicant's claimed system comprising a memory system, for serving the data storage needs of all the ports with the memory system being separated from the ports by access flow regulator functioning as an interface. This deficiency of Ferguson should be sufficient, by itself, to inventively distinguish Ferguson from independent claims 1, 2, and 17 as well as from any dependent claims reciting an access flow regulator and a common memory system serving the data storage needs of all ports.

In view of the above, the examiner's comments are in error regarding the claim 1 recitation of an excess flow regulator for generating request for the reading and writing of memories. The cited Ferguson material in column 41 lines 31 to 35 discusses nothing of relevance to applicant's invention.

Another inventive relationship set forth in many of applicant's claims including claims 1, 2, and 17 refers to the interplay between the RAM bank memories 1803 on figure 18 and the remote RAMs 1806. On memory write operations a large data file is extended by access flow regulator to a selected RAM 1803; the selected RAM 1803 stores a portion of the data file and transfers an excess portion of the data file via multiplexer 1808 to bulk memory RAM 1806. The process works in reverse on a memory write operation during which the requested data file is read out by transferring the contents of the selected RAM 1803 to the excess flow regulator and by concurrently transferring the portion of the file stored in bulk memory 1806 via the selected RAM 1803 to the access regulator.

The examiner cited the material in column 41 lines 31 through 35 of Ferguson as relevant to the above-discussed interplay between the RAMs 1803 and bulk memory 1806. The examiner is an error. A review of the material in column 41 lines 31 through 36 clearly shows that the referenced Ferguson material has no relevance whatsoever to the examiner's characterization or to the applicant's claimed invention. The reference material discusses the head and tail queue of buffer 318 on figure 3 of Ferguson and the notification area memory 319 on figure 3 of Ferguson. If the examiner would familiarize himself with the relevant material in Ferguson which describes the function of elements 318 and 319, he would learn that these two elements do not function as recited in the applicant's claims. Instead he would learn that memory 318 receives and stores only the head and tail portion of a buffer received from output request processor 306. The examiner would also learn that the remainder of the buffer is stored in notification area member 319. Memory 319 is as a bulk memory which stores the entirety of a received buffer except for the head and tail, which is stored in memory 318. In contrast to the applicant's claimed invention, Ferguson stores the head and tail portions of a receive buffer directly into memory 318 and stores the remainder of the buffer directly into memory 319. Ferguson does not store the entire buffer in memory 318 for subsequent transfer of an excess portion of the buffer to memory 319. This relationship between the applicant's high-speed RAM banks 1803 and bulk memory 1806 is crucial to the present invention. This relationship is recited in applicant's claims, but apparently is not understood by the examiner. The

Examiner also apparently fails to understand the distinctions between the Ferguson structure of figure 3 and applicant's claimed invention regarding the interplay between RAM banks 1803 and bulk memory 1806.

The examiner is in error with respect to his analysis of the last 2 recited elements of claim 1 wherein the first element in essence recites writing a first portion of a data file and said excess portion of said data file into said high-speed memory. The next claim element recites transferring said excess portion of said data file from said one high-speed memory to said bulk memory while leaving the first portion of said data file and said one high-speed memory. The cited portions of Ferguson, namely, column 41 lines 31- 35 and 57-60 do not disclose any material remotely resembling to anything in applicant's claims including claim 1.

It can be seen that the examiner's analysis and rejection of claim 1 relies on material in Ferguson and is not even relevant or material to examiner's assertion that Ferguson anticipates applicant's claim 1.

Re the rejection of claim 2 over Ferguson. This rejection is respectfully traversed. Claim 2 recites a method of operating a memory management system for reading out a data file priorly written into the memory management system. Claimed 2 recites many of the same elements and steps as recited in claim 1. Claims 1 and 2 are similar with the differences between them being that claim 1 is directed to a write operation while claim 2 is directed to a read operation of the same memory management system.

The examiner relied on essentially the same arguments in his rejections of both claims 1 in 2. The applicant's response and traverse regarding the regarding rejection of claim 1 is essentially the same as that priorly set forth for claim 1. Claim 2 also differs from Ferguson since Ferguson does not disclose a memory management system that is common to and serves the data storage needs of a plurality of ports of a file server with the ports being separated from the membrane management system by an access flow regulator functioning as an interface. Claim 2 also recites the interplay between the high-speed memory RAM banks 1803 and bulk memory 1806. Claim 2 also recites the manner in which a data file is read out by transferring the portion of the file in the bulk memory 1806 to the high-speed RAM 1803 which then extends the

remainder of the data file to access flow regulator 1801. Ferguson fails as in anticipation of his recitation for the same reasons as priorly discussed in connection with claim 1.

Re: the rejections of dependent claims 3 and 4. The rejection of these dependent claims over Ferguson is respectfully traversed since these claims should be allowable has being depended upon allowable independent claim 1. Also, the rejection of these dependent claims is further traversed since the material in Ferguson cited by the examiner as being relevant had been reviewed and found to be of no relevance to the patentability of dependent claims 3 and 4.

Re: the rejection of independent claim 17 over Ferguson. This rejection is respectfully traversed. Claim 17 is an apparatus claim directed to both a write and read operation for a memory management system that is coupled by an access flow regulator functioning as an interface to data ports of a file server. The merits of the examiner's rejection of claim 17 over Ferguson need not be discussed in detail since, as accurately noted by the examiner, claim 17 is a combination of claims 1 and 2. The rejection of claim 17 need not be discussed further since the same arguments in comments set forth by the applicant in connection with claims 1 and 2 are hereby incorporated by reference in this traverse of the rejection to assert that Ferguson fails to anticipate independent claim 17 for the same reasons priorly discussed with regard to claims 1 and 2.

Claim rejections-35 U.S.C. 103

The applicant respectfully traverses the 35 U.S.C. 103 rejections of dependent clams 5-16 and 18. The first ground for traverse is that all of these dependent claims are either directly or indirectly dependent upon an allowable one of independent claims 1, 2, or 17. A second ground for traverse is that these rejections fail to establish a prima facie case of obviousness containing evidence of a motivation to combine the references. The examiner merely asserts that references could be combined. His assertions are based on 2020 hindsight using information gleaned from a reading of applicant's disclosure and using this information against the applicant to support an assertion of obviousness. The examiner's methodology in formulating a 103

obviousness rejection involves the steps of: reading the applicant's disclosure and claims to identify necessary search descriptors; feeding the search descriptors into the USPTO search engine; receiving the outputs of the USPTO search engine; combining these outputs into groups to formulate assertions that it would be obvious to combine the prior art identified by the search outputs; and applying these assertions to the applicant's claims.

Examiner is reminded that sections 2142 and 2143 of the MPEP state that the fact that references could be combined does not prove obviousness; also, the fact that it might be desirable to combined references does not prove obviousness. The MPEP requires that motivation to combine must be found in the reference itself. Accordingly, the examiner is respectfully requested in the next office action to indicate with particularity and specific where such motivation is to be found in Ferguson for each obviousness rejection made by the examiner. The examiner is also requested to state exactly what element in Ferguson he proposes to alter to incorporate an element of a patent of the combination relied on by the examiner. Since Ferguson makes extensive use of block diagram disclosures, it is not sufficient in a 103 rejection to make a broad-brush assertion that something could be modified or combined. Specifics are required by the applicant so that he can fully understand how the examiner proposes to redesign Ferguson to meet the created combination of references relied upon by the examiner.

Ferguson and the other references are complex references and it is respectfully submitted that fairness to the applicant requires that the examiner provide sufficient information regarding is proposed combination to enable the applicant to understand the merits of the rejection and to provide a meaningful response. This requires information indicating what element in Ferguson needs to be modified or replaced by an element in the other references. The unsupported assertion that two patents could be combined to reject the applicant's claims conveys no useful information and is unfair to the applicant. The undersigned cannot meaningfully respond to such rejections until the examiner provide information indicating what element of each patent is to be used in the combination and how each such element is to be modified.

Dependent claims 5, 6, 13, 16, and 18 were rejected under 35 U.S.C. 103 (a)

over Ferguson in view of Brigati (US 6,279, 068). This rejection is traversed since these claims are believed to be allowable as being dependent upon an allowable one of amended independent claim (1, 2, or 17). These rejections are also traversed since the examiner of did not indicate what element in Ferguson would require replacement or modification to incorporate Brigati.

The rejection of claim 5 is further traversed since the cited combination of references (Ferguson and Brigati) discloses nothing of interest to claim 5. Ferguson does not disclose an access flow regulator that meets the requirements of the presently claimed access flow regulator which, in independent claim 1, functions as an interface between a file server and a memory management system. Also, nothing can be found in the cited references corresponding to the recited state controller of claim 5. The examiner apparently considers Ferguson element 316 to be the state controller. This cannot be since, on figure 3 of Ferguson, element 316 is not individual to a high-speed memory. The cited material in column 2, lines 24-27 of Brigati is directed to a memory operation that uses the time during which a first memory is busy with a task to select another memory to carry out a read or write operation. No such function is recited in claim 5. Therefore the examiner's comments regarding his cited art and applicant's claim 5 cannot be understood.

At a lower level of detail, the examiner discusses Ferguson on the lower portion of page 8 with regard to the steps of claim of 5 that are not disclosed by Ferguson. Then, at the top page 9, the Examiner cites Brigati as disclosing the steps of operating an access flow regulator to select an idle high-speed memory and transmit said write request from access flow regulator over said request buss to the state controller to select a high-speed memory. The examiner asserts that Ferguson further discloses operating state controller to extend write request to high-speed memory. The examiner's arguments cannot be understood. The cited material in Brigati is directed to the efficient use of a pair of memories and their selection. This material in Brigati has nothing to do with the steps of applicant's claim 5. In particular, Brigati does not disclose an access flow regulator having the attributes and characteristics of applicant's access flow regulator; namely, that the access flow regulator as it is an interface between applicant's memory management system and a file server.

The rejection of claim 6 over Ferguson in view of Brigati is respectfully traversed. It is submitted that dependent claim 6 should be allowable as being indirectly dependent on allowable independent claim 1. Claims 6 is directed to a process of determining occupancy level of a high-speed memory, transmitting a request to the high-speed memory if the occupancy of the high-speed memory is not exceeded and redirecting the request to bulk memory if the present occupancy level of the high-speed memory is exceeded. Also, Ferguson does not disclose structure comparable to applicant's access flow regulator whose details are characterized in the independent claim is 1, 2, and 17. Ferguson has been studied and found to be of no relevance. Ferguson does not disclose an access flow regulator or the process of determining the occupancy level of a high-speed memory, transmitting a request to the high-speed memory if its occupancy level is not exceeded, and redirecting the request to a bulk memory if the occupancy level of the high-speed memory is exceeded. Brigati was not discussed by the examiner in the rejection of claims 6. The applicant is therefore similarly sees no need to discuss Brigati.

The rejection of claim 13 over Ferguson in view of Brigati is respectfully traversed. Claim 13 has been studied together with the examiner's argument in support of this rejection. Ferguson and Brigati, taken is singularly or in combination, do not disclose structure equivalent to applicant's in bulk memory which, as defined in the independent claims, is part of a memory management system that serves the storage needs of all ports of a file server but it is separated from a file server by means of an access flow regulator functioning as an interface between the memory management system and a file server. Dependent claim 13 is also believed to be allowable as being indirectly dependent upon allowable independent claim 1.

The rejection of claim 16 over Ferguson in view of Brigati is traversed for the same reasons set forth for claims 5, 6, and 13. The examiner cites paragraph 17 of Brigati. This reference is meaningless since the applicant has no idea what material in Brigati the Examiner identifies as paragraph 17. The text in Brigati is not identified by paragraph numbering. Ferguson and Brigati have been studied and found to contain no method or apparatus of interest to the method recited in claim 16. Neither Ferguson nor Brigati, taken is singularly or in combination, disclose structure equivalent to

applicant's access flow regulator and applicant's high-speed memories which has characterized in the independent claims comprise part of a memory system separated from but common to all ports of a file server.

The rejection of claim 18 over Ferguson and Brigati is also respectfully traversed. The examiner relied on this comments for claims 16 and 17 in his rejection of claim 18. The examiner's comments are confusing since claim 17 is an independent claim and was discussed together with independent claims 1 and 2 in the 35 U.S.C. 102 rejections. It is therefore assume that the examiner's statement is in error and that the examiner meant to refer only to claim 16. This rejection of claim 18 is traversed for the same reasons primarily discussed with regard to the rejection of claim 16. Both Ferguson and Brigati are of no interest with respect to claim 17 neither discloses structure comparable to in having the attributes of applicant's access flow regulator or high-speed memories.

Dependent claims 9 and 12 were rejected under 35 U.S.C. 103 (a) over Ferguson in view of Milway US 6,470,428. This rejection is traversed and the claims 9 and 12 are believed to be allowable as being depended upon an allowable independent claim (1, 2, and 19). This rejection is further traversed since the examiner's analysis of Ferguson does not contain elements corresponding to all elements of the rejected claims. The Examiner also presented no evidence indicating how his proposed combination could be achieved or what element in Ferguson would require replacement or modification to incorporate Milway.

Claim 9 in essence recites the method of reading out a bulk memory to a high-speed memory in a burst mode. Claim 9 of further recites reading out a high-speed memory for transfer to an access flow regulator. Neither Ferguson and/or Millway taken either singularly or in combination disclose anything of relevance to the method of claim 9. Two examples of this deficiency will suffice. First of all, neither reference discloses the readout of a bulk memory to a high-speed memory and a burst mode. Secondly, neither reference discloses the readout of a high-speed memory to an access flow regulator having the characteristics of the access flow regulator recited in the independent claim 2 upon which claim 9 is dependent.

Dependent claim 12 is distinguishable from the cited references for the same

reasons as it is dependent claim 9. Neither reference discloses the control of the transfer of a data file from a high-speed memory to a bulk memory having a lower speed. Also, neither reference discloses the controlling of the transfer of a data file from a bulk memory of a lower speed to a high-speed memory.

Dependent claim 11 was rejected under 35 U.S.C. 103 (a) over Ferguson in view of Brigati and in further view of Klikki US 6,868,061 (hereinafter Klikki). This rejection is traversed since the claims are believed to be allowable as being depended upon an allowable independent claim 1. The examiner presented no evidence indicating how his proposed combination could be achieved. He presented no description of what element in Ferguson would require replacement or modification to incorporate Brigati and Klikki as he proposes.

The examiner's rejection of claim 11 cannot be understood. The examiner cites material in column 6, lines 51 through 54; and in column 7 lines 49 to 53; and in column 7, lines 45 through 49. In citing this material, the examiner neglected to identify which one of the three references contains the cited material. This failure by the examiner significantly increased the difficulty of attempting to identify the art relied upon by the examiner. The undersigned was forced to consider all three of the cited patents and try to guess which patent might possibly be relevant to each citation of a specified column and specified lines.

Claim 11 is directed to a method of determining an occupancy level for each request and in extending the request to high-speed memory if the occupancy level is not exceeded. Claim 11 also recites buffering a request in an access flow regulator if the occupancy level is exceeded. All three patents have been reviewed and none discloses anything of interest to the recited method of claim 11. In particular, it should be noted that the last step of claim 11 involves buffering a request in the access flow regulator. This limitation by itself should automatically distinguish claim 11 from any of the cited patents. None contains structure comparable to the access flow regulator recited in claim 11. The reason for this conclusion is that the access flow regulator of claim 11 is defined in claim 1 and is being an interface between a memory management system and a file server. None of the cited references, taken singularly or in combination, discloses an access flow regulator meeting the limitations of claim

11. In view of this, the rejection of claim 11 lacks merit and mean and need not be further discussed.

Dependent claims 7,8,14, and 15 were rejected under 35 U.S.C. 103 (a) over Ferguson and Brigati in further view of Lee et al US PG Pub 2004/0205305 (hereinafter Lee). This rejection is traversed because these claims are believed to be allowable as being depended upon an allowable one of amended independent claims (1, 2, and 19). This rejection is further traversed since the examiner's analysis of Ferguson does not contain elements corresponding to the elements of the rejected claims. The examiner presented no details indicating how his proposed combination could be achieved. He presented no description of what element in Ferguson would require replacement or modification to incorporate Brigati and Lee as he proposes.

The rejection of claim 7, 8, 14, 15 under 35 U.S.C. 103 (a) in view of Ferguson, Brigati, and Lee is respectfully traversed. A first reason for traversed is that all of these dependent claims should be allowable as being neither indirectly or directly dependent upon and allow although one of independent claim is one, 2, or 17.

These are rejections are further traversed since the cited art has been studied and none discloses apparatus of interest to that recited in the rejected claims. Briefly, all of claims 7, 8, 14, and 15 are directed in various degrees of specificity to the use of a multiplexer for the transfer of data files between the elements of applicant's memory system including a bulk controller memory, a high-speed memory, and a state controller. Claim 7 is generally directed to the use of the multiplexer for transmitting data files from state controllers to a bulk memory under predetermined conditions including a determination of whether they were requesting state controller is to be granted access to the bulk memory. This method is not shown in any of the cited references including Lee. Claim In 8 is dependent upon claims 7 and includes a further step of applying data from a high-speed memory and the state controller via a multiplexer to the bulk memory. This is not shown in any of the cited references. Claim 14 is dependent upon claim 7 and has the steps of using the multiplexer to determine which requesting high-speed memory is to be granted access to the bulk memory, granting access to one of the high-speed memory's and buffering the remaining requests in the high-speed memory. This is not shown any of the cited references

including Lee. Claim 15 is dependent upon claim 7 and contains the steps of using the multiplexer to determine the identity of a high-speed memory to which a data file is to be corrected by the multiplexer and controlling the transfer of the data file from bulk memory to the unidentified high-speed memory. This is not shown in any of the cited references including Lee.

Ferguson, Brigati, and Lee are complex references and it is respectfully submitted that fairness to the applicant requires that the examiner provides sufficient information regarding is proposed combination to enable the applicant to understand the merits of the rejection and to provide a meaningful response. This would require information indicating what element in Ferguson's needs to be altered modified or replaced by an unidentified element in Brigati as well as Lee. The unsupported assertion that the patents could be combined to reject the applicant's claims conveys no useful information and is unfair to the applicant.

Epilogue

It should be appreciated that many of the elements recited in dependent claims that are preceded by the use of the word "said" to indicate that the element was priorly recited in and one of independent claims 1, 2, or 17. Each element in a dependent claim preceded by the use of the term "said" requires that the recited element be interpreted to have all of the functions, limitations, and characteristics of the earlier recitation of the same element in an independent claim. The most notable example of this is the term "access flow regulator", which it is characterized in the independent claims as being an interface between a memory management system and the ports of a file server. The same comment can be made for other elements recited in the dependent claims. Such other elements include "bulk memory" and "high-speed memories". By virtue of the earlier recitation of these elements in an independent claim, the recitation of these memories in dependent claims shall be construed as being part of the memory management system. Such elements in the dependent claims shall be considered to be comparable to elements disclosed in a reference only if the element in the reference has all characteristics of the element in the applicant's independent claim that recites the element.

There are at least two main distinctions between the prior art and the methods and apparatus recited in the present claims. The first distinction is that the applicant's memory management system and applicant's memories are not provided on a per port basis as shown by Ferguson. Instead, the applicant's memory management system together with its memories are common to and serve the storage needs of a file server that is separate and distinct from applicant's memory management system. Applicant's access flow regulator functions as an interface between the memory management system and the file server. All of these distinctions compel the conclusion that Ferguson is as different from applicant's invention as night is different from day. A memory in Ferguson port of figure 3 is provided on a per port basis. A memory in Ferguson port of figure 3 is not common to all ports of Ferguson. The memories in the applicant's memory management system are not provided on a per port basis. Instead, they are common to all ports of the file server served by applicant's memory management system. This is a fundamental distinction of the between Ferguson and the applicant's invention.

Another significant distinction between applicant's invention and the prior art is the use by applicant of high-speed low capacity memories and low speed bulk memory together with the manner in which data is transferred on a write operation from the access flow regulator to the high-speed memory and, in turn, to the bulk memory. The process works in reverse on a read operation in which a file to be retrieved is read out of the bulk memory and applied via the high-speed memory to the access flow regulator.

The above discussed distinctions are breakthroughs in the art and distinguish the present invention from the known prior art.

It is respectfully submitted that the claims remaining in application are allowable over the prior art and such action is respectfully requested.

The examiner is respectfully requested to call if the prosecution of the application can be expedited by so doing.

Respectfully submitted,

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SIGNATURE OF PRACTITIONER
Donald. M. Duft, Reg. No. 17,484
Duft Bornsen & Fishman LLP
Telephone: (303) 786-7687
Facsimile: (303) 786-7691

Correspondence address:
Customer Number: 50525